ABSTRACT OF THE DISCLOSURE

An input digital video signal is allotted by a first multiplexer (310) between regions of a display area to be driven in a dividing manner and is sequentially input to a first memory portion (30A) or a second memory portion (30B). Each of the first and second memory portions (30A and 30B) comprises an input-side line memory (32) composed of, for example, 400-stage input side shift register to which said digital video signal is sequentially input, and an output-side line memory (34) for receiving the data transferred in parallel from the input line memory (32) to serially output the stored data from a selected one of output portions (Out1~4) provided at the 320th , 256th or first stage FF34. The output portion of the memory (34) is thus selected by selectors (380A, 380B) in accordance with the number of pixels in the horizontal direction of the LCD panel, such that LCD panels having the different numbers of pixels can be driven with the same structure. The output-side line memory (34) further includes a data shift direction switching circuit. By controlling the switching circuit and selecting the output at the first stage FF34(Out4) in the 400 stages, the data from the output-side line memory (34) can be output in the order opposite to the input order into the input-side line memory (32).